



H-780-02

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Appl. No. : 10/600,541 Confirmation No. 5764  
Applicant : T. SAKATA et al.  
Filed : June 23, 2003  
Title : SEMICONDUCTOR INTEGRATED CIRCUIT WITH MEMORY REDUNDANCY CIRCUIT  
TC/AU : 2133  
Examiner : J.D. Torres  
Customer No. : 24956

**AMENDMENT**

**MAIL STOP: AMENDMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed May 2, 2006, please amend the above-identified application as follows:

**Amendments to the Claims** are reflected in the listing of claims which begins on page 2 of this paper.

**Remarks/Arguments** begin on page 5 of this paper.